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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,394	12/28/2001	Jum Soo Kim	054216-5016	2075

9629 7590 07/23/2003

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EXAMINER

NGUYEN, KHIEM D

ART UNIT PAPER NUMBER

2823

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/029,394

Applicant(s)

KIM ET AL.

Examiner

Khiem D Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☐ Other: ____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features as recited in present claim 7, lines 11-15 must be shown or the feature(s) canceled from the claim(s).

No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

Claim 7 is objected to because of the following informalities: In claim 7, lines 18, after “, and a code address memory cell is formed”, delete “is” and insert “in”. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 1-2 and 4-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Shirai (U.S. Patent 6,482,697).

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In re claim 1, Shirai discloses a method of manufacturing a code address memory cell, the method comprising the steps of:

forming a gate insulating film (FIG. 5L, 108) in which a plurality of oxide films and nitride films are stacked on a semiconductor substrate (FIG. 5L, 101);

forming a polysilicon film (FIG. 5L, 111) on the gate insulating film;

etching given regions of the polysilicon film and the gate insulating film to form a gate (col. 15, lines 46-62); and

performing an impurity ion implantation process to form a source region (FIG. 5L, 103S) and a drain region (FIG. 5L, 103D) (col. 14, lines 27-40).

In re claims 2 and 4, Shirai discloses wherein the gate insulating film (FIG. 5L, 108) is formed by stacking at least two or more layers of at least one of the oxide and nitride (oxide-nitride-oxide (ONO)) film (col. 15, lines 38-42).

In re claims 5 and 6, Shirai discloses wherein the gate insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shirai (U.S. Patent 6,482,697) as applied to claims 1-2 and 4-6 above.

In re claim 3, Shirai discloses wherein the polycrystalline silicon film and the gate insulating film have a thickness of (0.22 micrometers \cong 2200 Angstrom) but fails to explicitly disclose wherein the gate insulating film has a thickness of about 30 ~ 300 Angstrom as recited in present claim 3. However, there is no evidence indicating the thickness range of the gate insulating film is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

3. Claims 7-8 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Shirai (U.S. Patent 6,482,697).

In re claim 7, Shirai discloses a method of manufacturing a code address memory cell, the method comprising the steps of:

forming a device isolation film in a give region on a semiconductor substrate to define an active region and a device isolation region (FIG. 5A, 102);

defining the active region into a cell region and a peripheral circuit region a given process;

forming a tunnel oxide film (FIG. 5B, 105) and a first polysilicon film (FIG. 5B, 106) on the entire circuit and then patterning the tunnel oxide film and the first polysilicon film so that the tunnel oxide film and the first polysilicon film can only remain in a given region of the cell region, thus defining a floating gate (col. 13, lines 3-8);

forming an insulating film (FIG. 5L, 108) in which an oxide film and a nitride film (col. 15, lines 38-42) are stacked on the entire structure to form a second polysilicon film (FIG. 5L, 107, 111);

patterning the second polysilicon film and the insulating film so that they can remain only in a given region of the cell region and the peripheral circuit region (col. 15, lines 46-51), thus forming a control gate in the cell region and a gate in the peripheral circuit region (FIG. 6); and

performing an impurity ion implantation process for a given region of the semiconductor substrate to form a source region (FIG. 5L, 103S) and a drain region (FIG. 5L, 103D) (col. 14, lines 27-40), so that a flash memory cell is formed in the cell region, and a code address memory cell is formed in the peripheral circuit region (FIG. 6).

In re claims 8 and 10, Shirai discloses wherein the gate insulating film (FIG. 5L, 108) is formed by stacking at least two or more layers of at least one of the oxide and nitride (oxide-nitride-oxide (ONO)) film (col. 15, lines 38-42).

In re claims 11 and 12, Shirai discloses wherein the gate insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shirai (U.S. Patent 6,482,697) as applied to claims 7-8 and 10-12 above.

In re claim 9, Shirai discloses wherein the polycrystalline silicon film and the gate insulating film have a thickness of (0.22 micrometers \cong 2200 Angstrom) but fails to explicitly disclose wherein the gate insulating film has a thickness of about 30 ~ 300 Angstrom as recited in present claim 9. However, there is no evidence indicating the thickness range of the gate insulating film is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
July 1, 2003


Gik Chaudhri
Supervisory Patent Examiner
Technology Center 2800